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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,423	03/07/2002	Yusuke Kawaguchi	220471US2S	8868

22850 7590 02/03/2003

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ALEXANDRIA, VA 22314

EXAMINER
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ERDEM, FAZLI

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 02/03/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/091,423

Applicant(s)

KAWAGUCHI ET AL.

Examiner

Fazli Erdem

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 03 August 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7,9-15,20,21,26,27 and 30 is/are rejected.
- 7) ☒ Claim(s) 2,4,6,8,16-19,22-25,28 and 29 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

### Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413) Paper No(s) \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Allowable Subject Matter***

1. Claims 2, 4, 6, 8, 16, 17, 18, 19, 22, 23, 24, 25, 28, and 29 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 9, 10, 14 and 15 rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (6,280,569) in view of Baliga (5,998,833) further in view of Korec et al. (6,285,060).

Regarding Claims 1, 9, 10, 14 and 15, Chang et al. disclose a high power unipolar FET switch which has an N- drift layer; a layer of metal contacts the drift layer via an ohmic contact to provide a drain connection for the FET. Each switch cell has a pair of trenches recessed into the drift layer and separated by a mesa region. Oxide layers line the walls and bottom of each trench, which are each filled with a conductive material; the conductive material in each trench is connected together to provide a gate connection for the FET. A shallow P region extends from the bottom of each trench into the drift layer and around the trench corners. A layer of metal

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contacts the mesa region via an ohmic contact to provide a source connection for the FET. The structure preferable operates as a “normally-off” device, with the potentials created by the work function difference between the conductive material and the N- mesa region completely depleting the mesa region. A positive gate voltage undepletes the mesa regions, creates accumulation channels adjacent to the oxide sidewalls of the trenches and modulates the mesa region thereby turning the switch on and allowing current to flow between drain and source via the mesa region and the accumulation channels. Chang et al. fail to disclose the correct gate and the trench structure, and correct epitaxial layer structure. However, Baliga discloses power semiconductor devices having improved high frequency switching and breakdown characteristics where the required trench and the gate structures are shown. Furthermore, Korec et al. disclose a barrier accumulation-mode MOSFET where the correct epitaxial layer structure is shown.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required trench and the gate and the epitaxial structures in Chang et al. as taught by Baliga and Korec et al. respectively in order to have a power semiconductor device having better performance.

3. Claims 3, 5, 7, 11, 12, 13, 20, 21, 26, 27 and 30 rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (6,280,569) in view of Baliga (5,998,833) in view of Korec et al. (6,285,060) further in view of Singh et al. (5,831,288).

Regarding Claims 3, 5, 7, 11, 12, 13, 20, 21, 26, 27 and 30, Chang et al., Baliga, and Korec et al. combination disclose all the claimed subject matter except they fail to show the thickness and the doping concentration of the epitaxial layers. However, Singh et al. disclose a

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silicon carbide metal-insulator semiconductor field effect transistor where the thickness and the doping concentration of the epitaxial layers are shown.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the thickness and the doping concentration of the epitaxial layers in Chang et al., Baliga, and Korec et al. combination as taught by Singh et al. in order to have a power semiconductor device with better performance.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE  
January 25, 2003

NATHAN J. FLYNN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800